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RM-7083

B. E. III (Sem. VI) (ECC) Examination

May / June – 2010

Computer Architecture & Organization

Time : 3 Hours] [Total Marks : 100

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 6) (ECC)**

Name of the Subject :

☛ **Computer Architecture & Organization**

☛ Subject Code No. : **7 0 8 3** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Draw flowchart or block diagram wherever it is necessary.

(3) Make necessary assumptions if required.

SECTION - I

1 (a) Answer the following: **(10)**

(1) The operation code must consist of at least _____ bits for a given 2^n operations.

(a) n-1 (b) n (c) n^2

(2) Define: microinstruction

(3) "Zero address instruction can be used in stack organized CPU". State true or false.

(4) Write the full form of MIMD.

(5) Write the microoperation for STA instruction.

(6) The next address generator is sometimes called a _____.

(7) The three major components of CPU are register set,ALU and _____.

(8) "The theoretical maximum speed up that a pipeline can provide is k that is number of segment".State true or false.

(9) In _____ mode, the operands are in registers that reside within the CPU.

(a) Direct (b) Register (c) Register Indirect

(10) The transformation from an instruction code into a control memory address is known as _____.

1 **(b)** **(1)** A computer uses a memory unit with 256K words of 32 bits each.A binary instruction code is stored in one word of memory.The instruction has four parts:an indirect bit ,an operation code,a register code part to specify one of 64 registers and an address part. **(6)**

(a) How many bits are there in the opcode,the register code and the address part?

(b) Draw the instruction word format and indicate the number of bits in each part.

(c) How many bits are there in the data and the address inputs of memory?

(2) Write down major characteristics of CISC processor **(4)**

2 **(a)** Explain interrupt cycle in detail with flow-chart. **(8)**

(b) A computer has 16 registers ,an ALU with 32 operationsand a shifter with 8 operations. All connected to a common bus system. **(7)**

(1) Formulate a control word for a microoperation.

(2) Specify the number of bits in each field of the control word.

(3) Show the bits of control word that specify the microoperation:
R4←R5+R6

OR

2 **(a)** Convert the following infix statements into reverse polish notation. **(8)**

(1) A*B+C*D+E*F

(2) A*B+A*(B*D+C*E)

(3) A+B*[C*D+E(F+G)]

(4) $\frac{A*[B+C*(D+E)]}{F*(G+H)}$

(b) Explain microprogram sequencer in detail. **(7)**

3 **Attempt Any Three:** **(15)**

(1) Explain Flynn's classification.

(2) Explain overlapped register window.

(3) (a) Draw a space time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

(b) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.

(4) An instruction is stored at location 200 with its address field at location 201.The address field has the value 500.A processor register R1 contains the number 400.Evaluate the effective address if the addressing mode is (a) direct (b) immediate (c) relative (d) register indirect (e) indexed with R1 as the index register.

(5) Explain four possible hardware schemes that can be used in order to minimize the performance degradation caused by instruction branching.

SECTION - II

Q.4 (a) Answer the following :

1. What is the function of memory management unit? 1
2. What is the use of valid bit in cache memory? 1
3. What is comparison method for binary division? 2
4. Why is biased exponent? 1
5. What transmission type uses start bits? 1
   a. synchronous b. broadband c. asynchronous d. baseband
6. What is aging registers? 1
7. What is Nonvectored interrupt? 1
8. What is cycle stealing in DMA? 1
9. Define: page fault. 1

Q.4 (b) Explain with flowchart restoring method of division. 8

Or

(b)Explain with flowchart multiplication of binary integers in signed 2's complement representation. 8

Q.5 (a)Explain Associative memory. 8

(b) What is DMA? Explain DMA transfer in a computer system. 6

Or

(a) Do following: 8

1. The access time of a cache memory is 100ns and that of main memory 1000ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9; a write through policy is used.
   A. what is the average access time of the system considering only memory read cycles?
   B. what is the average access time of the system for both read and write requests?

2. An address space is specified by 24 bits and the corresponding memory space by 16 bits.
   A. how many words are there in the address space?
   B. how many words are there in the memory space?
   C. if a page consists of 2K words, how many pages and blocks are there in the system?

(b)Explain with flowchart CPU- IOP Communication. 6

(c) Explain handshaking method of asynchronous data transfer. 2

Q.6 Attempt any four of the following : 16

1. Explain 2-bit by 2-bit array multiplier and give specifications for j × k array multiplier.
2. Explain segmented page mapping.
3. Explain parallel arbitration.
4. Differentiate between tightly coupled and loosely coupled systems.
5. Explain Daisy-chaining priority interrupt.